What is claimed is:

1. An interconnect comprising:
a pad; and
at least two vias coupled to the pad.

2. The interconnect of claim 1, wherein at least one of the at least two vias is formed substantially beneath the pad.

3. The interconnect of claim 2, wherein at least one of the at least two vias is coupled to the pad by a conductive segment having a first end having a first width and a second end having a second width, the first end being connected to the at least one of the at least two vias and the second end being connected to the pad, and the first width being less than the second width.

4. The interconnect of claim 2, wherein the pad has at least five substantially straight edges and the at least two vias comprise three vias and only two of the three vias are coupled to the substantially straight edges.

5. The interconnect of claim 4, wherein at least one of the only two of the three vias coupled to the substantially straight edges is coupled to one of the substantially straight edges through a tapered conductive segment.

6. A circuit substrate comprising:
a substrate;
a first pad formed on the substrate, the first pad coupled to a first potential plane;
a second pad formed on the substrate, the second pad coupled to a second potential plane by at least three vias; and
a capacitor coupling the first pad to the second pad.

7. The circuit substrate of claim 6, wherein at least one of the at least three vias is formed substantially beneath the second pad.

8. The circuit substrate of claim 6, wherein each of the at least three vias is formed substantially beneath the second pad.

9. The circuit substrate of claim 8, wherein the capacitor comprises high frequency capacitor.

10. The circuit substrate of claim 9, wherein the capacitor comprises a ceramic capacitor.

11. A circuit substrate comprising:

a substrate;

a pad having a bottom surface, the pad formed on the substrate and the bottom surface being in contact with the substrate; and

at least three vias coupled to the bottom surface.

12. The circuit substrate of claim 11, wherein the pad comprises a substantially square core pad having four edges and three non-square pads, wherein each of the three non-square pads is located adjacent to one of the four edges and is contiguous with one of the four edges.

13. The circuit substrate of claim 12, wherein at least one of the three non-square pads comprises a substantially triangular pad.

14. The circuit substrate of claim 13, wherein the substantially triangular pad is coupled to one of the at least three vias.

15. The circuit substrate of claim 12, wherein each of the three non-square pads is coupled to one of the at least three vias.

16. A method of forming an interconnect, the method comprising:

forming at least two vias in a substrate; and

coupling each of the at least two vias to a pad.

17. The method of claim 16, wherein coupling a pad to each of the at least two vias comprises:

directly coupling the pad to at least one of the at least two vias.

18. The method of claim 17, further comprising:

forming a tapered conductive segment on the substrate to couple at least one of the at least two vias to the pad.

19. The method of claim 18, further comprising:

electrically coupling an integrated circuit to the pad.

20. The method of claim 19, wherein electrically coupling an integrated circuit to the pad comprises:

inserting a solder element between the integrated circuit and the pad.